MICROTAPE MANUAL

SECTION 1

SYSTEM SUMMARY

Microtape provides the flexibility, speed, and storage capabilities of magnetic tape while maintaining the convenience of paper tape. Its size and portability, in addition to the reliability obtained by the tape format and track head arrangement, render its integration into overall systems an easily accomplished task. The Microtape system described in this manual consists of a Type 550 Microtape Control unit and a Type 555 Dual Microtape Transport Unit. This system is used with either a PDP-1 or PDP-4 to provide a fast, convenient input-output device.

MICROTAPE CONTROL TYPE 550

The Microtape Control Unit 550 is a program break control. That is, it allows the transfer of information word by word between the computer and the Microtape Transport Unit 555. Since the control does not deal with blocks of information from the tape, words can be individually read and written within certain general limits. Since the computer is required to attend to the needs of the control on a word by word basis, however, more of its time is spent in handling the needs of the control than would be the case if the control were of the block transfer type.

The Microtape Control Unit 550 contains electronic circuitry necessary for performing the logical and timing functions essential to the operation of the system; the Microtape transport unit contains the tape handling elements, the drive mechanism, and relays for switching the tape heads onto a master bus system.

MICROTAPE TRANSPORT TYPE 555

Operation of the Microtape transport is, normally, controlled by an associated computer. However, manual control is also afforded, by means of the controls located on the front panel of the unit. A description of each control on the panel is included in Section 3 of this manual.

A maximum of four tape transport units (eight drives) may be controlled by the Type 550 Control Unit by means of the mark track, which gives format information to the control, and the program interrupt facility of the PDP-4 and 1. The computer is permitted to do computation in the main program during tape operations. Information is transferred with programmed checking by means of the subroutines supplied, but these routines do not allow simultaneous computation during word transfers since these programs are general purpose and take most of the computer's time for their operations.

USES OF MICROTAPE

Microtape is particularly suitable for certain applications. Some of these are covered briefly below.

Storage

The first application is simply as a storage device for programs and data. Since the tape handling is extremely simple, it is easy, and in fact desirable, to store the program on Microtape and simply carry it to the computer when needed. To carry the same amount of data on either cards or paper tape would be unwieldy to say the least. Different library tapes can be changed easily, if necessary, and retrieval of any portion of the tape is relatively fast.

Editing

If modifications to the programs are necessary, the tape need not be either rewritten entirely to preserve the order, or added to at the end. The program can be read in, modified, and rewritten in the same location on the tape if its block length is not changed. This indicates also that many programs can be written utilizing a minimum number of drives.

On-Line System Data Handling

On an on-line system, use of individual Microtapes to store information keyed in by individual users provides a fairly cheap and efficient way of handling data. The ability to multiprogram during searching (which requires by far, the greatest amount of time) means that more than one individual can have access to the computer without appreciably affecting internal processing, and without causing an inordinate amount of waiting time for the user. An extension of this is discussed in the next application.

Since the Microtape reel is only 3-1/2 inches in diameter, and the system can read or write in both directions, random access to any point on the reel is relatively fast. A fairly large amount of data can be stored, however. For example, one tape can hold more than 22 complete 4K memories. In a real-time, multiple-user, random access system, many tapes can be moving simultaneously even though data can be transferred on any one tape at a time. For example would be a system with several remote Teletypes, each of which requires random access to information stored on several Microtapes. When the first request occurs, the program can place the appropriate tape in search mode and begin searching for the block. If another request occurs, the program can note approximate position of the first tape in relation to the block requested, select the new tape (leaving the old tape moving) and start searching for the new block. A programmed clocking device or timing loop can be used to determine when

to reselect the first tape, check for the correct block, and transfer the data. As new inquiries enter the system, a queue can be formed with the request for the nearest information and the time needed to reach it at the top of the queue. As information is found, the clock is reset to the time necessary to reach the next request and so on.

In this way, multiple requests for information on a single tape can be easily handled if both records can be found by searching in the same direction. There are times, of course, when data is reached on more than one tape simultaneously. In this case, the tape searching for the later request can either be stopped before the record is reached or can be turned around if the record has been bypassed. In terms of overall time to the user, very little difference will be noticed. Of course if two separate Microtape controls are used, data can actually be transferred on more than one tape simultaneously, if the program is fast enough to react to the various flags.

Sampling of Data

A fourth type of application involves the continuous movement of the tape. There are many instances when it is desirable to store sampled data on a tape for future analysis by other programs. Memory fills up rapidly, however; and during the time information is transferred onto the tape, sampling is usually stopped to avoid synchronization problems. Thus, the information stored usually consists of data relating to many relatively short samples. With Microtape, one whole tape can be written with one command, and therefore an extremely long sample of fairly rapid data can be achieved. If desired, the entire tape can be considered as one long block of information. Storing of informations from an analog-to-digital converter would be a logical use of such a system.

SPECIFICATIONS

Listed below are the physical and electrical characteristics of the combined 550 and 555 Microtape Unit. All values are approximate.

HEIGHT	12 inches
WIDTH	19 inches
WEIGHT	65 pounds
TAPE AND REEL	260 feet of 3/4 inch tape on a 3-1/2 inch reel. Tape is 1.0 mil Mylar.
WORD TRANSFER RATE	One 18-bit word each 200 (±10) microseconds. Bit rate is constant when moving forward. Although velocity varies slightly, bit density changes serve to maintain a constant bit rate due to the constant rate timing track. In reverse direction the variation in time between words becomes ±20% depending on location along the tape.

TAPE SPEED	80 inches per second
DENSITY	375 (±60), 3-bit characters per inch. 3 million bits per reel.
START TIME	200 milliseconds
STOP TIME	150 milliseconds
TURN AROUND TIME	300 milliseconds
START AND STOP DISTANCES	8 inches
ACCELERATION	700 (±150) inches per second
BLOCK SIZE	Arbitrary segments of any length determined by format control tracks.
NUMBER OF HEADS	10 heads to read or write 5 channels. Each channel is duplicated for reliability purposes.
TRACK DUPLICATION	Pair of tape heads, wired in series, associated with 2 identical tracks. The polarity of the analog sum of the voltages from the individual heads of the pair determines the correct value of the bit.
MOVEMENT OF TAPE	Accomplished by reciprocal voltages applied to the motors driving the spools. These voltages control the torque of each motor.
COMMAND SIGNAL LEADS	Contact closures, Select, Go, Reverse and 10-wire select bus. One 2-wire write interlock loop. Two connector plugs wired in parallel.
INFORMATION SIGNAL LEADS	Five shielded triplets
POWER REQUIREMENTS	115 volts 60 cps, 1.5 amps
TAPE HEAD EFFECTIVE GAP WIDTH (READ)	600 (±100) microinches
TAPE HEAD EFFECTIVE GAP WIDTH (WRITE)	500 (±100) microinches
WRITE CURRENT	100 milliamperes
READ SIGNAL	5 millivolts p-p, minimum

FEATURES

The general features incorporated in the Microtape system are: bidirectional reading and writing; Manchester type polarity sensing; prerecorded mark and timing tracks; pretested subroutines; individually addressable blocks; and in the sense explained elsewhere in this manual, individually addressable words. The simplified mechanical construction of the Microtape transport yields good reliability at the expense of quick stops and starts.

Recording Technique

Most of the above features are the result of the type of recording technique used in the system (Manchester, or polarity sensed). Briefly, this technique utilizes a change in magnetic flux

for every data bit on the tape. Of importance in this technique is the direction of each flux change. A "negative-going" change represents a 1; a "positive-going" change is 0. The polarity of the voltage generated by these flux changes is sensed to determine the type of bit written at a particular location on tape. A timing track is recorded on the tape for purposes of strobing the data tracks. The timing strobe is issued to coincide with the maximum rate of change in flux of a data bit, thus at the point of maximum read voltage.

Preprogrammed Subroutines

Information is transferred with programmed checking by means of the subroutines which may be obtained from Digital. There are three types of subroutines currently available. The first is a basic set of subroutines for searching, reading, and writing. The second, called Microtog, is a set of maintenance and diagnostic programs entirely under control of toggle switches on the main computer console. The third, called Microtrieve, is a routine which permits the saving of programs or data on Microtape, with a quick retrieval feature using toggle switches. A more detailed description of these programs is included at the end of Section 2.

FORMAT

Microtape uses a ten track recording head to read and write five duplexed channels. The five tracks actually written consist of the timing track, used to strobe the other tracks; the mark track, used to raise flags in the program, create sequence breaks, detect block mark numbers, and protect control portions of the tape; and three data tracks. An 18-bit word therefore uses six slots of three bits each on the tape.

Tape Skew

Some tape systems strobe on the first bit of a slot, then impose some arbitrary delay after which all signals present are read. This produces problems since differences may occur in the two directions. Variations in tape speed between write time and read time would result in non-compensated changes in the necessary delay. In the Microtape system the redundant heads are placed in a relationship to each other which, eliminate most of the cross-talk between the most important tracks. This relationship also places the timing tracks at the edges of the tape so that strobing on the analog sum of the timing track signals guarantees that the data tracks are read when they are in the most favorable position. The data tracks are placed in the middle of the tape where the effect of skew is at a minimum.

Timing and Mark Tracks

The heart of the Microtape system is the prerecorded timing and mark tracks. It is necessary to understand the meaning of the word "prerecorded." At present, one of the programs pro-

vided with the Microtape system (1-127 IO) writes the timing track and block format desired for the individual user. The Microtape system includes a programmed mode of operation called "write timing and mark track" and a manual switch which both permits writing on the timing and mark tracks and also activates a clock which produces the timing track and flags for program control. Unless both the mode and the switch are used simultaneously, it is physically impossible to write on the mark or timing tracks. A red indicator lights on all transports connected to the appropriate control when the manual switch is in the "on" position. In this mode only, information channel "one" (high order bits 0-5) is also connected to the mark track channel. Therefore, in one pass of the tape, the timing track, mark track, block format, and block mark numbers are created. Since part of the data word must be reserved to produce the mark track, it is impossible to write intelligent data in the information channels at the same time. For this reason also, only 12 of the 18 bits are used for block mark identification, and bits 0-5 must be ANDed out when checking block mark numbers. (See Figure 6 for format of bits on the tape.) Once the format has been recorded, the user is able to use the Microtape system for actual data storage.

The actual mark track which is written on the tape (see Figure 2) was selected after careful consideration and provides many functions not readily discernible at a casual glance. Some of these are listed below

Program synchronization
Block end detection
Error checking and prevention
Protection of control information
Block and word addressability
Automatic bidirectional compatibility
End of tape detection
Variable block format
Inclusion of marks to allow expansion for more automatic systems of the future.

For complete understanding of the questions of program synchronization and block and detection, Figures 2 through 6 should be studied closely, using the explanation which follows to clarify certain main points.

Modes of Operation

There are three main programmed modes of operation which require that the user either provide information to the Microtape system or accept information from the Microtape system. These are the search, read, and write modes. A fourth mode, move, simply moves the tape without supplying or requesting information. In order to indicate to the programmer that

the system is ready to transfer information, certain flags are raised. When these occur, the programmer must either load new information to be written, or unload information just read, and must do so within a specified time to prevent loss of information and error indications. If the program interrupt mode is being used, the raising of any of the flags mentioned also causes a break in which the individual flags must be interrogated.

In order to produce these flags, the mark track is read by passing the bits through an 8-bit "moving window" which shifts bit by bit as the tape moves. A decoder associated with the window interprets the pattern present, and raises the appropriate flags, if necessary. An 8-bit window is used, even though each mark is six bits long, to provide greater reliability, since a mark will not be recognized as ligitimate unless the last two bits of the previous mark were legitimate. This is one of the reasons which requires ordering of the marks on the tape. Note that whether the program is reading or writing, the mark and timing tracks are always being read.

Search Mode

In the search mode the data flag is raised only when a block mark is read (see Figure 3). The program must unload the buffer within 53 milliseconds, and bits 6-17 contain the block mark number. Bits 0-5 contain the mark code.

Write Mode

In write mode, the Microtape system automatically writes the reverse check sum and raises data flags when it requires information to be written on the tape (see Figure 5). The first data flag requests the first data word of the block, and the last data flag requests the last data word of the block; therefore there are a total of 256 data flags for a 256 word block. Note that the program loads each data word as the Microtape system is writing the previous one; thus a flag is raised requesting a data word when it has just passed the place on the tape two words ahead of where the word is to be written. Compare this with read mode discussed below. Time between data flags is approximately 200 microseconds. When the prefinal mark is detected, a block end flag is raised which accomplishes two things. First it is a request for the program to load the calculated check sum (normally the complement of the 18-bit ring sum of the reverse check sum and the data words); and second, it allows the program to detect that a block has been completed without the use of any programmed counters. After the check sum is written, the writers are turned off to avoid any possibility of destroying the control portion of the block. Approximately 1.2 milliseconds are available to switch to search mode if a check of the next block mark number is desired. If the control remains in write mode, the Microtape system writes the next reverse check sum and raisesthe next data flag after approximately 1.6 milliseconds.

Read Mode

In the read mode the first data flag is raised when the reverse check sum has been read (see Figure 4). The reason for this becomes obvious since a block may be read in either direction independent of the direction in which it may have been written. The first word read, therefore, sets the register which the program uses to accumulate the check sum. Each successive data flag indicates that a data word has been read and should be unloaded from the buffer, stored in memory, and accumulated in the check sum. When the check sum mark is detected, a block end flag is raised, indicating both the end of the block and that the check sum is in the buffer. This word would normally be unloaded and added to the accumulated check sum producing a total of zero. Any other result indicates that the tape has been read incorrectly, and the programmer has the option of continuing in any manner desired.

When reading, there are 256 data flags for a 256 word block, and each flag states that the associated data word is in the buffer. In the present system, validity checks on the data portion of the tape are done by program control only. As a matter of fact, if for some reason a check sum is not desired, the check sum word can be used as simply another data word.

Checking of Mark and Timing Tracks

Checking of the mark and timing tracks is accomplished through the hardware and the physical characteristics of the mark track itself. One check, that of checking the last two bits of the previous mark, has already been mentioned. However, another interesting fact emerges from what happens as the tape passes by the mark detecting window, bit by bit (see Figure 6). Close examination shows that unless the window is actually looking at a legitimate mark on the tape (except on end mark), the bits in the window differ by at least two bits from any possible legitimate mark. (In the rare instance where they are only one bit different, the window has been cleared for other control purposes, so that one bit can make no difference at all.) This guarantees that a 1-bit error any place on the mark or timing tracks can not cause an erroneous mark to be detected. It also allows checking for asynchronous marks. For example, once the window is in synchronization (normally by passing over a block mark), a mark track error is indicated and the error flag raised if a legitimate mark is found in less than six shifts of the window or if a legitimate mark is not found after each six shifts of the window. These combinations of checks make it virtually impossible to misinterpret the mark track and thereby destroy information.

Nothing in the system prohibits the changing of modes at any time during the movement of the tape. However, care should be taken to include the difference in counting words when switching from read to write or from write to read, the recovery of the read amplifiers after writing (about two word times) and the fact that writing in various locations in the block

invalidates the check sum at end of the block. Within those limits almost any combination of modes can be used; and because of the polarity sensed recoding technique, even individual words can be replaced.

Complement Obverses

One other unique feature of the mark track is that the six control marks before the data marks are, what we have chosen to call "complement obverses," of the six control marks after the data marks. The complement obverse of a word is defined as the complement of a word with the bits read in the reverse direction, for example:

010110 (26) and 100101 (45)
001000 (10) and 111011 (73)

The data mark is the complement obverse of itself. When reading in the reverse direction, the flux reversals on the tape are opposite to those when reading forward and the bits are read in the reverse order. Therefore, the mark track window sees exactly the same thing in both directions.

BidirectionalAbility

With one exception, no special logic is required to distinguish the format of the tape in either direction. The one exception involves the shifting of information into the Microtape buffer. Since the assembling of the 18-bit word is done by the hardware, it is necessary to shift the buffer in opposite directions for opposite movement of the tape in order to present words to the computer as they were originally written. This means that if a record is read opposite to the way in which it was written, each 18-bit word appears in the buffer exactly as it originally appeared in memory; however, the last word written would be the first one read, etc.

The end marks on either end of the tape illustrate this bidirectional ability even better. As the end marks are complement obverses of each other, only recognized is that end of tape which will physically come off the reel if further movement continues. Again, no special hardware is needed for opposite ends of the tape, and there is no harm in coasting into or turning around in the end zones. Errors are indicated only if attempting to go further into the end zone. The particular bit structure of the end marks is a repetitive one, so that any shift of three bits in the window appears as another end mark. This makes it virtually impossible to pull the tape off the reel in any of the normal modes. Sensing of the appropriate end mark stops the tape and raises the error flag if the tape is in any of the normal modes.

There are only two "abnormal" modes. One is the write timing and mark track mode, mentioned previously, in which no marks can be detected since they are being written. The other

is the case where a tape has been left moving but not connected to the control (deselected). In this case, only the marks on the actually selected tape are recognized. In only these two circumstances can the tape be pulled off the reel.

Block Size

Therefore, although the blocks are structurally alike in terms of the types of marks on the mark track, they need not contain the same number of data words. Indeed every block on the tape can be of different length, if such a format was created originally. The system will operate in the manner outlined no matter what the length of the block. One other feature exists which may prove useful, especially in the future designs. If for any reason the distance between blocks must be lengthened, it can be done simply by adding "01" codes between the reverse block mark of block N and the forward mark of block N+1 (see Figure 6). Since the pattern "01010101" already appears at the junction of the two marks, it may be continued indefinitely without harm.

Additional flexibility has been retained for future expansion. For example, in the future the contents of the lock mark might be used to determine if the block is "file protected," that is, cannot be written on. The final mark could be used to request the check sum from the hardware in a system having automatic sum checking, etc.

SECTION 2

OPERATING INSTRUCTIONS AND PROGRAMMING

The operating instructions for the Microtape system consist, basically, of tape loading and manual switching operations. Each is described below. Following them is a subsection devoted to programming information.

LOADING THE PROGRAM

There are no special instructions other than the ones for using the computer. There are, however, some standard pitfalls. First be sure the program is the correct one for the computer as well as for the desired operation. Insert the paper tape in its proper orientation. There is one correct way out of four. If the program does not load (in the case of a PDP-4), check the loader instructions. Remember that if it is an 8K machine add 010000 to all instructions other than IOT's. Then follow the written program closely.

LOADING THE TRANSPORT

To load the transport with a full spool of tape, proceed as follows. Make sure that the shiny side of the tape is wound face out from the hub, or spindle hole, of the spool. During threading, keep the shiny side of the tape up. First, place the spool over the left hand spindle and press in until the spool is firmly seated on the spindle. Thread the tape over the tape guides, and over the tape heads (see Figure ____.) Insert the free end of the tape down against the interior hub of the empty take-up spool. Make sure the tape end touches the hub. The power switch should now be turned on. The electrostatic created by the turning of the empty spool is sufficient to cause the free end of the tape to be taken up and automatically wound about the spool hub, effectively completing the threading process. After the tape has been so threaded, allow the spools to continue rotating for approximately two seconds. During this time, observe the spools for possible wobble and correct if present. Always use Certified tape. Other tape may contain defects which will cause problems from the start.

Certified Tape

Microtape systems give the user, for the first time, a means of "certifying" or marginal checking his own tape. Certifying is done by recording a pattern on tape, reducing the signal read from the head by a factor of five, and making sure that the tape still works. This process assures that, for the conditions at the time of the test, there was an amplitude margin of at least five to one for the signal from the tape. The attenuation is accomplished by replacing a jumper plug on the back panel of the control (at C19 and C24) with another which has a resistor attenuator on it. The module number of the jumper plug is 1033.

DEC can provide certified tape. This tape has written on it a mark track, a timing track, and a pattern of 577 blocks each 256 words long. It has been checked as above with the further refinement that read amplifiers of average gain margins were used and the signal was attenuated to an average of 1.6 millivolts peak to peak. When ordering a certified tape, include the serial number of the 550 control unit.

SWITCH FUNCTIONS

WRTMR switch is located just below plug A22 on the 550 Control. Its function is to turn on the clock which is used only when writing the timing and mark track on the tape.

SELECTOR switch is the 8-position switch located on the 555 Control Panel. The number to which the switch is set becomes the unit number of that particular drive.

WRITE LOCK switch has three functions. Off turns the 115 VAC off to the motors. Write-Lock allows the 550 control to command any mode except write. The Write position allows the control to write information either in the data channels or mark and timing channels depending upon the program used.

The FWD-REV switch manually controls the motion of tape.

Turning Off Unit

Ordinarily, the Microtape system is controlled by an associated computer which turns the system off. When off, the tape should be checked for excess slack, and corrected, if necessary, by using the AC switches which control the individual drives. If computer control is not provided, the Microtape unit can be turned off by simply throwing the power switch.

PROGRAMMING

Included at the end of this subsection are IOT's of relevance when the Microtape system is used in conjunction with a PDP-1, PDP-4, computer.

Preprogrammed Subroutines

As mentioned earlier in this manual, three types of program subroutines are furnished with, or can be obtained for use with, the Microtape system. The first is a basic set of subroutines for searching, reading, and writing. The second, Microtog, is a set of maintenance and diagnostic programs which can accomplish combinations of Microtape functions using the toggle switches on the console. The third, Microtrieve, is a routine which saves programs or data on Microtape and permits quick retrieval by means of toggle switches on the computer console. Microtog and Microtrieve both employ the basic read, write, and search subroutines described above. These latter subroutines, with small differences are basically the same for both the PDP-1 and PDP-4.

Subroutines for PDP-1

For the PDP-1, the basic subroutines are designed to read or write one block of information in either direction, depending on the position of the tape and the direction in which the tape is searched. Searching in the reverse direction results in a transfer of data, the start of which coincides with the end of the block in core storage. In the forward direction, data is transferred upon encountering the beginning of the block in question. Thus, the direction of reading is independent of the direction of writing, and memory words are preserved. In searching, the appropriate unit designation, the block number, and the error return are used as parameters. The read and write subroutines both require a unit designation, block number starting address, and error return as parameters. The read and write subroutines automatically enter the search subroutine to find the request block.

After completion of the subroutines mentioned above, the tape is not stopped, but allowed to run if so programmed.

Subroutines for PDP-4

Subroutines applicable to the PDP-4 permit specification of the total number of words for transfer regardless of block format. Searching is permitted in both the forward and reverse directions, however, both reading and writing are permitted only in the forward direction. Should the number of words specified for transfer result in use of only a portion of some block, the remainder of the block would be filled in with zeros (if writing) or the remainder of the block would be read (if reading) even though the words so read are not utilized in any manner. The purpose of this latter action is to permit the check sum to be calculated or checked. It should be noted that the program interrupt mode of operation constitutes the basis for the above discussion, and that one auto-index register is defined by the main program. The instruction dismis is defined as a jmp to the instructions which dismis the interrupt. Instructions to check the appropriate flags are also included in the interrupt sequence.

For the PDP-4, the search subroutine requires a unit designation, block number, and error return as parameters. Searching terminates with either a stop, or a running in either the forward or reverse direction, according to the subroutine entrance used. As soon as searching is started, a return is made to the main program to allow simultaneous multiprogramming.

For the read and write subroutines, the unit designation, block number, starting and ending core addresses, and error return are required as parameters. These routines cause automatic entry into the search mode to position the tape. During data transfers, no multiprogramming is permitted. After completion of transfer, the tape is stopped. Errors are detected, coded numerically, saved in status bits, and indicated by a special return. The coding of the error type may be followed by continuance of the desired program.

Microtog

The Microtog subroutines are applicable for use with either the PDP-1 or PDP-4. These subroutines consist of a number of short programs which check out the various Microtape functions, under the control of the console toggle switches. Some of these short programs are: creating the mark track as individual block format; reading or writing specific portions of the tape; writing a clear tape in either direction; sum-checking specified modes for indicated times or distances, generation of specified types of data blocks, and exercising the tape by writing, reading, and sum-checking in both directions. Errors are analyzed and indicated by typeout. The typeout includes the block causing the error and the exact status of the Microtape at the time of the error.

Microrieve

The Microrieve subroutine permits, by use of toggle switches on the main console, the storing or retrieving of data in specified locations. During storing, a search is made for the block indicated; then the indicated area of memory is written on the tape, accompanied by an identification designation into control words. Upon completion of the storage process, a typeout is executed. The typeout lists the starting and ending block numbers used for the storage and a number representing the total check sum of the entire area so written.

During retrieving, a portion of data information on the tape is stored in core memory. Its location is indicated by the status of the toggle switches. For retrieving, the unit designation and block number must be specified; the control words on the tape indicate the starting address and length of information in memory. In this subroutine, the check is made to insure that the block specified is actually the start of the storage area. Upon completion of retrieval, a typeout is effected which lists the starting and ending block numbers and the total check sum. These items can be checked against the typein data as a verification of the retrieval. Errors

are analyzed as noted above under Microtog.

Instructions

Input-output transfer instructions for use when Microtape is employed with a PDP-1 or PDP-4 are given in Tables 3-1 and 3-2. Table 3-3 gives a sample of Microtape operation with a PDP-4.

MICROTAPE INSTRUCTION LIST

PDP-1 Mnemonic	PDP-1 Binary	PDP-4 Mnemonic	PDP-4 Binary	Function
mrd	720501	mmrd	707512	READ. Clears I/O or AC and transfers one word from MMIOB to bits 0-17 of I/O (PDP-1) or AC (PDP-4).
mwr	720601	mmwr	707504	WRITE. Transfers one word from bits 0-17 of I/O (PDP-1) or AC (PDP-4) to MMIOB
mse	720301	mmse	707644	SELECT. Connects the unit designated in bits 2-5 of the I/O (PDP-1) or AC (PDP-4) to the Microtape control.
mlc	720401	mmlc	707604	LOAD CONTROL. Sets the Microtape control to the proper mode and direction from bits 12-17 of the I/O (PDP-1) or AC (PDP-4), as follows: Bit 12 = Connect (Go) Bit 13 = Reverse Bit 14 = Spare Bits 15-17 = Mode: 0 = Move 1 = Search 2 = Read 3 = Write 4 = Spare *5 = Read through block ends *6 = Write through block ends *7 = Write timing and mark track I.e. 42 = Read forward 62 = Read reverse 43 = Write forward 41 = Search forward 61 = Search reverse

* Not presently connected.

TABLE 2-2 MICROTAPE INSTRUCTION LIST (continued)

PDP-1 Mnemonic	PDP-1 Binary	PDP-4 Mnemonic	PDP-4 Binary	Function
mrs	720701	mmrs	707612	READ STATUS. Clears the I/O or AC and transfers the Microtape status conditions into bits 0-8 of the I/O (PDP-1) or AC (PDP-4) as follows: Bit 0 = Data flag Bit 1 = Block end flag Bit 2 = ~~Error flag~~ MISS Bit 3 = End of tape Bit 4 = Timing ~~error~~ Bit 5 = Reverse Bit 6 = Go Bit 7 = Mark track error Bit 8 = Tape unable
		mmdf	707501	Skip on Microtape data flag In search mode: Block mark number should be unloaded via (m) mrd instruction In read mode: Data or reverse check sum should be unloaded via (m) mrs instruction In write mode: Data should be loaded via (m) mwr instruction.
		mmbf	707601	Skip on Microtape block end flag. In read mode: Unload forward check sum via (m) mrd instruction. In write mode: Load calculated forward check sum via (m) mwr instruction.
		mmef	707541	Skip on microtape error flag. Timing error, mark track error, end tape, or tape unable condition has occurred. Use (m) mrs instruction to detect specific error.

NOTE: mmse and mmlc clear the error flag; and mmse, mmlc, mmrd, and mmwr clear the data and block end flags.

TABLE 2-3 MICROTAPE OPERATION CHART (PDP-4)***

FLAG	MOVE MODE	SEARCH MODE
Data flag cleared on mmrd mmwr mmlc mmse This flag causes interrupt.	No data flags raised. Tape motion is continuous until end marks are sensed at far end of tape.	Data flag means that the MMTOB contains a block number. Write mode may be specified within 400 microseconds to transfer the block. Read mode may be specified within 600 microseconds.* Any other mode (including stop), may be commanded at any time. Transfer of block number must be completed in 53 milliseconds to avoid a MISS.**
Block Flag cleared on mmrd mmwr mmlc mmse This flag causes interrupt.	Should not occur.	Should not occur
Error flag cleared on mmse mmcl (also clears MISS, END, MTE This flag causes interrupt.	Error flag means that an error has occurred. An mmts command will load AC bits 0–8 with status information. (END is only possible error.) END status bit is set when tape reaches far end. Error flag is raised. Tape stops.	Error flag means that an error has occurred. An mmts command will load AC bits 0–8 with status information. (END, and MISS are only possible errors.) End status bit is set when tape reaches far end. Error flag is raised. Tape stops. Miss Status bit is set when a data or block flag has not been cleared from previous use.

* All times are nominal for forward direction. In reverse direction add ±20%.
** MISS indicates a programmed timing error; i.e., information will be lost (missed) because the routine is taking too long to transfer data to or from the buffer.
*** Operation for the PDP-1 is similar except that the I/O is referenced rather than the AC.

TABLE 2-3 MICROTAPE OPERATION CHART PDP-4 (continued)

FLAG	READ MODE	WRITE MODE
Data flag cleared on mmrd mmwr mmlc mmse This flag causes interrupt.	Data flag means that MMIOB contains a data word. An mmrd must be given within 200 microseconds for data transfer. First data flag in block indicates reverse check sum. Change to other modes possible within 200 microseconds. If write mode is desired, a 1-word delay occurs after mmwr is given.	Data flag means that MMIOB is ready for data word. An mmwr must be given within 200 microseconds for data transfer. Initial (-0) check sum is written automatically. First flag in block is a request for first data word. Change of mode possible within 200 microseconds. Since tape system is bidirectional the initial check sum written must be placed at either forward or reverse check sum location in block, depending only on direction commanded.
Block flag cleared on mmrd mmwr mmlc mmse This flag causes interrupt.	Block flag means that check sum is in MMIOB. First data flag of next block automatically occurs in 1.4 milliseconds. Change to search mode must be made in next 800 microseconds in order to catch next mark. Change to write mode must be made within next 1.2 milliseconds in order to start new block (not recommended - Block number should be checked by search mode).	Block flag means that check sum should be loaded into MMIOB with an mmwr. First data flag of next block occurs in 1.6 milliseconds. Change of mode commanded at last data word (D_{256}) is delayed while check sum is written. Change to search mode must be made within 1.2 milliseconds to read next block number. Preferred method of stopping is to change to search mode, then check succeeding block number for correctness before stopping.
Error flag cleared on mmse mmlc (also clears MISS, END, MTE) This flag causes interrupt.	Error flag means that an error has occurred. An mmrs command will load AC bits 0-8 with status information. (END, MISS, mark track error (MTE) are only possible errors.) End status bit is set when tape reaches far end. Error flag is raised. Tape stops. Miss status bit is set when a data or block flag has not been cleared from previous use. Mark track error (MTE) status bit is set upon discovery of certain mark track and timing track errors.	

SECTION 3

THEORY OF OPERATION

ENGINEERING DRAWINGS

All the microtape prints are fully cross referenced. The numbers shown in parentheses on the block diagram refer to the block schematic print numbers and geographical references as follows: The first two characters (EM, IN, C2, C1, etc.) indicate the mnemonic title of the appropriate block schematic, and the second two characters (B4, C2, etc.) indicate where on the named print the reference is made. The letter indicates the vertical dimension, which is shown on the right and left hand margins; and the number indicates the horizontal direction, which is shown across the top or across the bottom. The destinations (or origins) of all signals are shown within the block schematics. If a given signal goes to two places, both at the same geometrical print location, this location is indicated twice. In this way a section of the wiring list can be built up for purposes of detailed troubleshooting or corrections to the hardware. Wiring lists are not maintained once the machinery is shipped.

MICROTAPE SYSTEM

The basic block diagram of the microtape system is shown in D-550-0-BD. At the top of this diagram, a horizontal line representing information and control plugs 0J1 and 0J2 serves to separate the computer (above) from the Microtape system (below). Another horizontal line located at the bottom of the diagram, representing the information bus plugs at C21, 22 and the control bus at B3, 4, serves to separate the tape drive mechanism (below) from the control system above it. The purpose of this diagram is to depict the inter-relationship of major signals utilized in the Microtape system. Some of these signals are shown as input-output transfers (IOT's). These are located at the top of the diagram, and are designated as being relevant to either the PDP-1 or PDP-4 computer. Input-output transfers without such designations are common to both computers. Thus, the IOT MMRD as shown is common to both computers; whereas the IOT MMEF is relevant only to the PDP-4.

Data Transfers

Information transfers are routed to or from the accumulator (AC) if a PDP-4 is used, or to or from the input-output buffer (IO) if the PDP-1 is used.

Data transfers between computer and tape are via the in-out register and the shift register in the control unit, as shown at the left of the diagram (D-550- -BD). From the AC or I/O of

the computer, information flows to the tape through 18 lines which connect the AC or I/O to the in-out register. These lines are one-directional only; a binary one is indicated by a ground on a line.

Information from the tape is forwarded to the AC or I/O from the in-out register of the control unit by means of another set of 18 lines; a one is indicated by -3 on a line.

A transfer of information between the in-out register of the control unit in the shift register is accomplished by a double set of 18 lines. Information flow between these registers is accomplished by simultaneous pulsing their in-gates by means of an interchange pulse. During writing, the contents of the shift register are transferred to the tape through the write amplifiers and tape heads; during reading, information is transferred from the tape through the read amplifiers to the shift register. A detailed discussion of the shift register, in-out register, and read and write amplifiers is included later in this section.

CONTROL FUNCTIONS

The basic control functions of the control unit are listed below. The titles of the block schematics which contain the indicated circuitry are shown in parenthesis.

Reading of timing track. The bits on the timing track are read and transformed into timing pulses which control the sequence of microtape operation. (TM).

Reading of mark track. The mark track is read and decoded to obtain flag signals, sequence breaks, mark numbers, and block ends. (W).

Transfer of information. Signals are generated to denote the direction of information exchange between the computer and the microtape. Information to or from the computer is transferred in parallel form; information to or from the tape itself is transferred in serial form. (IN).

Generation of control responses. The timing pulses (tp), the marks, and the mode of operation (read, write, search, etc.) are used to generate proper control responses (flags, shift signals, interchange pulses, etc.). (62, TM). Memory of mode, selection, and motion commands of the program are shown in (C1).

Reading of Timing Track

The basic timing pulses (TP1 and TP0) are derived from the timing tracks of the tape. TP1 is generated during the negative-going zero-crossings of the timing track voltages picked up by the tape heads. Tape head voltages, appear as sign waves. The zero-crossings of the voltages picked up by the head are transformed by the read amplifier into square waves, the transitions of which occur in synchronism with the zero-crossings of the original head voltages. The read amplifiers, which have high and uncontrolled gain, saturate at any input signal over 100 micro-volts peak-to-peak.

Timing pulse TP1 marks the time the change in direction of flux of the data or mark bits is at maximum, and therefore ready for transfer to storage registers. During writing it is used to write the flux reverse which represents the bit. Timing pulse TP0 denotes between-bit time, that is, the appropriate time to shift into the writers the next bits that are to be written. In effect, TP0 designates the time that the head is passing through the boundary region between bit locations on the tape.

Another timing pulse designated as TP2 is obtained by delaying TP1 approximately 4.5 microseconds. TP2 is used to check mark track information picked up by the TP1 preceding it. The time interval between TP1 and TP2 is sufficient to allow CO gates to set up. In effect, TP2 commands an inspection of the control word (if any). TP0 is sometimes used to accomplish the same thing.

Timing pulses TP0, TP1, and TP2, after being generated, are gated with various other signals. One such signal is the delay in progress (DIP) signal, which is in effect whenever the proper tape speed is in the process of being attained, whenever turn around of the tape is occurring, or whenever the process of tape transport selection is being carried out. During such times, timing track information is considered to be invalid insofar as proper operation of the system is concerned.

In addition to the above, the timing pulses undergo gating to reduce the effect of cross talk during writing. Such gating introduces a delay after actual origination of 10 microseconds for any TP signal mentioned above. After gating (or before gating) the time lapse between TP1 and TP0, or between TP0 and TP1, is 15 microseconds.

The OFF level occurs whenever the GO flip-flop is clear, provided that the write enable flip-flop (WREN) is in the ZERO state. This AND function of the write enable signal is to prevent the timing pulses to continue even though the GO signal may be present.

Relay Timing and Mark Signal

The relay timing and mark signal (RELTM) functions to suppress timing pulses picked up from the tape during this mode of operation. In addition, the RELTM signal enables the timing and mark track writers and physically connects them to the TT and MTS, it also starts the WRTM (write timing and mark load clock). In addition to the above, the RELTM signal lights a red lamp on the drivers.

The clock mentioned in the paragraph above drives a gray code c unter which, in turn drives the track writers and generates quadrature phase TP pulses by means of the same pulse amplifiers which normally buffer the timing pulses. It should be noted that the TT writers are switched at times which are in quadrature with the timing pulses this ensures the preservation of the relationship between the negative-going, zero-crossing of a timing signal and the coincidence of the flux reversal of the data or mark bit.

Reading the Mark Track

The mark track is read in the same manner as are the information or data tracks. That is, timing pulse TP1 loads the first flip-flop of a shift register from the (push pull) outputs of the read amplifier. This occurs at the time of maximum flux reversal of a data or mark bit passing under the head. This same flux reversal was previously written on the tape by means of the same TP1 — during an earlier writing operation — now under consideration. Since the head senses maximum flux reversal at TP1, an accurate output is obtained from the associated read amplifier. It should be mentioned that the direction of the flux change determines the polarity of the read amplifier output, hence the kind of bit being read — one or zero. An inspection of Figure ____ discloses the relationship between flux directions and binary value as recorded on the tape.

Unlike the data words, which are routed as described above between tape and computer, the mark track bits are routed only to the control unit. In the control unit, the mark track bits are shifted into the window register. This 8-bit register always holds the last eight bits read from the mark track. Each new reading of a new mark track bit shifts the register so that the new bit is shifted in, and the old eight bit shifted out. Since mark track bits are read in succession, there is a succession of shiftings of the window register. After each shift however, the window register accurately reflects the last 8 bits read from the mark track.

Window Register

The outputs of the flip-flops of the window register are fed to a group of AND circuits. The function of these latter circuits is to detect particular patterns as they appear in the register. Any particular pattern of bits in the register remains such only for a period of approximately 33 microseconds; at the end of this time, the next TP1 pulse shifts the register, to create (possibly) a new pattern. Accordingly, the AND circuit outputs can be asserted only for 33 microseconds. Thus, after the mark track heads read into the window register a particular pattern as created by the last bit read, the AND circuits, fed by the register, are allotted a time interval of 33 microseconds in which to recognize the pattern and produce the appropriate responses.

The AND circuits are comprised of diodes which drive inverters. The circuits are arranged so that any particular inverter output is at ground whenever its associated flip-flop in the register is enabled. (During the writing of timing and mark tracks, the RELTM signal is used to inhibit the shifting of the window register to prevent the accidental detection of marks during this process.)

Although referred to as an 8-bit register above, the window register stores a ninth bit which, although not part of the pattern fed into the AND gates, serves to control the accurate reading

of marks during starting or when switching to a running transport. Bit 9 is set into the register on a shift pulse only if bit 8 is a 1. Bit 9 is cleared by the clear window pulse, which clears all other flip-flops in the register. When not present, bit 9 prohibits operation of the AND circuits into which the window register feeds. When present, bit 9 enables these circuits.

The importance of bit 9 resides in its power to prohibit the reading of mark track patterns until the proper conditions are met. Thus, at the start of the mark track reading process, after clearing of the window register, a one from the mark track must be shifted through the window register, to position nine in the register in order that a pattern (bit arrangement) in the register may be detected by the AND circuitry mentioned above. In this way, bit 9 prevents partial patterns from being erroneously detected. (Other circuits also function to prevent erroneous detection: these circuits clear the entire window register when activated.)
The patterns or bit arrangements presented by the window register to the AND gates for detection are six bits long. The window register itself holds eight bits. The ninth bit, although forming a part of the register, is in no way utilized by it in the pattern detection process. Because of this circuit configuration, the window register is capable of providing 8-bit patterns; the order of code patterns is fixed in the shift register patterns. The 8-bit pattern capability utilizes the last two bits of the preceding pattern.

MSY Register

The window register and the associated decoding circuitry do not completely decode the mark track patterns. To achieve complete decoding, the MSY register circuit is used. The function of this MSY register is to decode the four blockstart marks (LOCK, REV CHECK, D1, and D2), and the four block end marks (prefinal, final, check, and spare).

The MSY register is loaded when a block mark is detected. Loading of a MSY register consists of inserting the binary arrangement 1000 into the register. Each time a block start mark is detected, a shift in the MSY register occurs. This shift causes the initial one to travel down through the register as other ones follow it. Thus, the first shift would cause the register to read 1000; the second, 1100; the third, 1110; and the fourth, 1111. The MSY register states are ANDed with detected block start marks to obtain the initial four marks mentioned above.

The four block end marks also cause four shifts of the MSY register. However, zeros rather than ones are propagated or shifted down the register. In this case, the initial state of the register is 1111. At the first shift, the state of the register is 0111 ; at the second, 0011; the third, 0001; and the fourth, 0000. This last, or fourth, state is decoded during trouble-shooting procedures.

The shifting of the MSY register occurs at TP2. The block start and block end marks are detected between one TP1 and the next. As a consequence of this, the useful output of the mark detection circuitry considered as a whole occurs at TP2.

Writing the Mark Track

Mark track words furnished by the computer are written on the mark track of the tape when the Microtape system is in the RELTM mode. The WRTM command (a result of the computer-issued MMLC instruction) must also be issued to effect mark track writing. Normally, the writing of the mark track is initiated when the Microtape system is in the stop condition. This permits the delay inherent in start up, at which time the DIP signal is effective, to render the timing pulses from the local clock ineffective. In this way, flags normally raised by the timing pulses are kept absent.

Word Counter

After start up, data flags are raised automatically at each word time. These flags are raised by the EK (or word counter) circuit. This circuit consists of a ring arrangement of six flip-flops in which a single one is caused to circulate. At the issuance of each data flag, the computer loads the word to be written on the mark track into the IOB. The word remains in the IOB until issuance of the next flag request, at which time the word is shifted into the shift register. From the shift register it is transferred through the write amplifiers and tape heads to the mark track. Since the shift register is logically divided into three sections, the writing of a mark track is accompanied by an identical writing of data track number one.

MARK TRACK ERRORS

Mark track errors are detected, if present, as follows. There are specific marks which occur each sixth time the window register is shifted. By using these specific marks, an error check procedure based on verifying the passage of six timing pulses between each such specific mark is effected. Utilized for this procedure is the EK (word counter) used also in the mark track writing process.

The EK is present at the same time that a block mark is detected (at TP2). The EK is rotated by TP0's. After six such rotations, caused by six successive TP0's, the EK is returned to its initial condition. As each initial position is reached, a new specific block mark should also be present. Thus, assuming no error, the initial condition of the EK and the detection of a specific block mark should exist concurrently. Should the two not exist concurrently, an error has occurred.

Since the EK is shifted at TP0, and since the window register is shifted at TP1, the concurrency of the initial state of the EK and the existence of the specific block mark is valid only after TP1 is issued and only before the following TP0 is issued. Because of this, the concurrency is checked, or strobed (since it is in gate form) at TP2.

It should be noted that there are particular times during Microtape operation when any error checking procedure is superfluous. For instance, during search, errors obtained from portions of the tape not yet read or written are irrelevant. Similarly, in the RIM mode, the WRTM mode, and the MOVE mode, any MTE is also irrelevant.

For the above reasons, the negative (for error) output of the error detecting circuitry is clamped to ground and rendered inoperative unless a particular mode such as write, read, write all, or read all, unclamps it.

Indications resembling errors, but not errors as such, are eliminated by clearing the window register during their "presence". In this respect, the two areas on the mark track located near the block mark most resembling errors are suppressed.

During the interval of time which elapses between the start of tape operation and the attainment of proper tape speed, the synchronization signals for the EK are nonexistent. Thus, error-detection cannot be performed. The BMF flag is set by the block mark and is used to gate out MTE's detected during this period. The tape system, when in this condition, would normally be in the search mode, rendering error detection superfluous, as described above. However, when in this condition, the tape system may be in the read mode. The BMF flag is then cleared by the clear window pulses.

Transfer of Information

In addition to furnishing information for, or receiving information from, the tape, the AC or IO can also forward a portion of its contents to the control unit for purposes of control only. By means of IOT instructions, the computer is able to select a tape unit (1 out of a possible 8 plus zero, or no unit), direct the motion of the tape, and command one of several possible modes. The selection of a tape unit is controlled by the arrangement of bits 2 through 6 in the AC or IO. These bits are loaded into the selection register by the mmse instruction. A ground on any of these lines indicates a binary ONE.

Load Control Instruction - The mmlc instruction, or load control instruction, if formed by the arrangement of bits 12 through 17 in the AC or IO. These bits are transferred by means of six lines to the command logic circuitry and the motion control circuitry. This circuitry then translates the bit arrangement into a specific tape direction and a specific equipment mode (move, search, read, write, WRTM, read all, write all, and read in mode). A ground on any of these six lines represents a binary one. There are eight possible modes which can be commanded by the command to the logic circuitry.

Timing Pulses and Mark Track Information

Like the accumulator or IO, the tape can furnish information to the control unit for control purposes only. This information comes from the work and timing tracks and is not passed through to the computer as data information. Instead, it is routed to the timing pulse generator circuitry and mark detection network (and window register). The information so routed consists of the timing pulses and mark track information derived from the tape.

The timing bits from the tape are picked up from the bus which is connected to a particular timing track head by the selection circuits, fed through a read amplifier and forwarded to the timing pulse generator. This generates three timing pulses: TP1, TP2, and TP0. These timing pulses are forwarded to other circuits in the control unit.

Mark track information, picked up by the mark track heads, is forwarded to the mark detection network circuitry. In accordance with the information received the mark detection network circuitry issues signals signifying that one of the various mark codes written on the work track has just passed over the head.

Operating in conjunction with the timing pulse generator is the WRTM clock circuitry. The purpose of this circuitry is to write mark track information on the tape. Information is forwarded from the clock to the tape through a write amplifier.

Read Status Instruction

The Microtape control unit transfers non-data information into the AC or I/O by means of the mmrs instruction. Although the bits constituting this instruction are temporarily stored in the AC or I/O, they do not represent any part of the data work or words. As shown on the overall block diagram (D-550-0-BD), the six leads composing the MMRS consist of REV, GO, UNABLE MK TK ERROR, MISS, and END. The MMRS command also reads the three flag levels into bits 0-2.

Flags

Another major group of signal leads of importance in Microtape system operation are those generated by the flag response net circuitry. This circuit issues to the computer the data flag, block end flag, and error flag signals. In the PDP-4, these signals are used to produce a program break request, enable the skip logic, and are sent to the AC on a MMRS.

In the PDP-1, the data flag signal (MMDF) is an indication to the computer that a particular data word being read or written is assembled and ready for transfer. The block-end flag (MMBF) indicates to the computer to unload the check sum if reading, or to load the calculated check sum if writing — indications to which the computer can respond by issuing a MMRD

instruction or a MMWR instruction. An error flag (MMEF) indicates to the computer that one of four error conditions has occurred; accompanying this error flag signal is the MMRS format (described above) stipulating the type of error responsible for issuance of error flag.

Generation of Control Responses

In general, the timing relationships between the computer and the Microtape system is governed by the ordinary program break control function. That is, the computer selects the mode of Microtape system operation by furnishing it with a MMLC instruction; this instruction directs the Microtape system to search, read, or write. The Microtape system, in accordance with mode generates the flags appropriate to the mode. The generation of flags and other responses continues until the tape is stopped by command, the mode is changed, or the tape end is reached.

The Microtape System control is in large part based on actions caused by reading of the mark track. These actions consist in the main of the initiating flag signals. A block mark is detected each time the tape heads encounter the boundary between data words. Depending upon the type of mark detected, and the mode of operation, a flag signal is issued. For example, in the search mode, the data flag is issued if the block mark is detected at TP2. The block mark and the TP2 signal and its attendant flag cause issuance of the interchange pulse, which shifts data between the shift register and the in-out register.

Searching

In the search mode, block number codes as read from the tape are forwarded to the computer for comparison purposes. Such forwarding is accomplished by means of the interchange pulses which transfer the block number codes from tape to the in-out register. During search, such transfers occur every 53 milliseconds (for a 256-word block). Each block number code so transferred is accompanied by the data flag. Should the computer fail to recognize the data flag before the next raise data flag pulse is issued, an error flag signal is issued. This flag signal is generated by a CD gate which has as inputs the RDF signal and the DF signal. The output of this gate sets the miss flip-flop to the ONE state. The encountering of an end mark automatically sets the end flip-flop and the go flip-flop is reset, stopping the tape.

Writing

The commanding of the write mode by the computer results in the issuance of a data flag by the control unit to the computer. The purpose of this flag is to indicate to the computer that the in-out register is prepared to accept a word from the computer for writing on the tape. The computer that transfers the word to be written to the in-out register by means of a MMWR command. The MMWR command extinguishes the data flag. (The WDA level results of a ORing or the block start and data marks. This level appears when the write data flags are to be raised.)

After the computer, during write, has transferred a word into the in-out register, the word is then interchanged and shifted. This process requires between 140 and 480 microseconds, depending on speed and program timing. During this time, neither the stop mode nor the read mode can be commanded. Should the computer direct the writing of information exceeding a block length, the Microtape system responds by shifting to the reading mode (in the block end area), writing the reverse check sum, and raising the first flags: the Microtape system then reverts to the write mode and utilizes TPOs for shifting purposes in writing.

Since the command to stop writing is inhibited in the boundary register between the last data word and the check sum, any read command given during this time is temporarily held in abeyance. At the raising of the block flag (read mode), a minimum delay of 240 additional microseconds is necessary in order that a stop command be carried out.

Reading

Entry into the read mode is accompanied by the issuance of data flags signifying readiness of words for transfer to the computer. The data flags are generated by the RDA signals and the TP2 pulses. The RDA signals, in turn, are generated by the OR formed by combining of the D1, D2, data mark, prefinal, and final signals.

Data flags are lowered by the computer-issued MMRD signals. The MMRD signal strobes the word in the in-out register into the computer.

Switching from Write to Read Mode - In the read mode, any switching to the write mode while within a particular block cause the following to occur. The data flag (read mode) signifying the readiness of the word in the in-out register for transfer to the computer is lowered by an MMRD. Assuming an MMLC (write) is issued just prior to the transfer, the first word to be written in the new write mode is written in the third word space following the word space from which the last word was read. Switching from read to write within a block necessitates the loss of two word spaces, which are neither written into or read from. The first data flag raised after the switchover indicates that the last word read has been transferred to the computer, and that the second word to be written can be released by the computer.

There is an exception to the above: if the first word to be written after switchover occupies the last data word space in the block, an RBF is raised. Also, if the first word so written falls into the check sum word space, no flag is immediately raised; instead the next flag is issued at the start of the next block.

Any switching from write to read occurs in the boundary region following the last word loaded for writing. In this boundary region, a dummy flag signal is issued. However, this flag signal corresponds to no special action; this flag is lowered when the first flag for read is raised. Because of the switchover, no validity check of the first three or four words read is possible.

SECTION 4

INTERFACE

This section will be supplied at a later date.

SECTION 5

MAINTENANCE

Maintenance of the Microtape control and transport consists of procedures repeated periodically as preventive maintenance as well as corrective maintenance if equipment should malfunction. Maintenance activities require the items listed below in addition to standard hand tools, cleansers, and test cables and probes.

Test Instruments

1. Tektronix Scope
2. Type CA plug in
3. Type E plug in

Test Programs

Rocker
Exerciser
Microtog

PREVENTIVE MAINTENANCE

Preventive maintenance consists of tasks performed prior to the initial operation of the equipment and periodically during its operating life to ensure that it is in satisfactory operating condition. Faithful performance of these tasks will forestall possible future failure by correcting minor damage and discovering progressive deterioration at an early stage. Data found during the performance of each preventive maintenance task should be recorded in a log book. Analysis of this data will indicate the rate of circuit operation deterioration and provide information to determine when components should be replaced to prevent failure of the equipment.

Cleaning

Clean the exterior and the interior of the equipment cabinet using a vacuum cleaner or clean cloths moistened in nonflammable solvent.

Clean the head and guides with the proper solvent. These are such an Ampex Head Cleaner or Freon 5. Check condition of guides and head at regular intervals. Always handle the tape with care. Greases tend to destroy the magnetic coating and dirt is a common culprit when dealing with magnetic tape systems.

Visual Inspection

Visually inspect the equipment for completeness and general condition. Repaint any scratched

or corroded areas with DEC blue tweed paint number 5150-865 or DEC gray enamel number 3277-IR55. Inspect all wiring and cables for cuts, breaks, fraying, deterioration, kinks, strain, and mechanical security. Tape, solder, or replace any defective wiring. Inspect the following for security: switches, knobs, jacks, connectors, transformers, fan, capacitors, lamp assemblies, etc. Tighten or replace as required. Inspect all racks of logic to assure that each module is securely seated in its connector. Inspect power supply capacitors for leaks, bulges, or discoloration. Replace any capacitors giving these signs of malfunction.

Marginal Checks

Marginal Checks are performed to aggravate borderline circuit conditions within the control logic to produce observable faults. Therefore, conditions caused by marginal components can be corrected during scheduled preventive maintenance to forestall possible future equipment failure. These checks can be used as a troubleshooting aid to locate marginal or intermittent components, such as deteriorating transistors. By recording the level of bias voltage at which circuits fail, progressive deterioration can be plotted and expected failure dates predicted. Therefore, these checks provide a means of planned replacement. The checks are performed by operating the logic circuits from an adjustable external power supply, such as the DEC Type 730 Dual Variable Power Supply.

To perform the checks:

1. Set the +10 MC/OFF/-15 MC switch on the marginal-check power supply to the +10 MC position.

2. Adjust the output of the marginal-check power supply so that the MARGINAL CHECK voltmeter indicates 10 volts.

3. Start Microtape operation in a normal program or in a routine which fully utilizes the circuits in the rack to be tested. If no program is suggested by the normal system application, select an appropriate maintenance routine.

4. Set the top normal/marginal switch to the up position on the rack to be checked.

5. Decrease the volt marginal-check power supply output until normal system operation is interrupted. Record the marginal-check voltage. At this point marginal transistors can be located and replaced, if desired.

6. Start operation. Then increase the volt marginal-check supply output until normal operation is interrupted, at which point record the marginal-check voltage. Transistors can again be located and replaced.

7. Return the top normal/marginal switch to the down position.

8. Repeat steps 2 through 7 for the center normal/marginal switch on the logic rack being checked.

9. Set the +10 MC/OFF/-15 MC switch on the marginal-check power supply to the -15 MC position and adjust the output until the MARGINAL CHECK voltmeter indicates 15 volts.

10. Repeat step 3.

11. Set the bottom normal/marginal switch to the up position for the rack to be checked.

12. Repeat steps 5 and 6, then return the bottom normal/marginal switch to the down position.

13. Repeat steps 1 through 12 for each module rack to be tested.

14. Adjust the output of the marginal-check power supply to zero volts and set the +10 MC/OFF/-15 MC switch to the OFF position.

Maintenance Programs

Programs are available for detecting errors in the Microtape control and may be used with marginal checking. Microtog, consisting of five subroutines, is used with the PDP-4. The Microtape Rocker and Exerciser programs perform similar functions for the PDP-1. See Section 2 for a description of the maintenance routines.

Periodic Adjustment of Stop Time

A Microtape unit is commanded to stop by the action of energizing the stop relay. This relay has a single normally closed contact on it which carries the holding current to the go relay. Therefore, (after 15 milliseconds) the go relay drops out followed, after a delay, by the timer relay. The time between go and timer dropping out defines a "stop pulse" which is caused to drive the trailing motor and stop the tape. If this stop pulse is too long the drive reverses rather than stops, and if it is too short, the drive does not come to rest at all but rather coasts to a sluggish stop. The length of the stop pulse is determined by the charge on the capacitor in the filter network and by R2 which is in series with the timer relay coil. If the drive is only partially up to speed, a shorter stop pulse is desired. Otherwise the long stop pulse will cause a reverse rather than a stop. For this reason, the charging resistor, R1, is included so that the capacitor charges up at approximately the same rate that the drive picks up speed in the first place. The procedure for adjusting R1 and R2 is now outlined.

To perform the adjustment:

1. Run a program (soon to be provided in Microtog) which starts the drive and allows it to

run for one second or more, and then commands stop, followed by a pause of one second and another run period of one second or more in the opposite direction. This program then causes the tape to rock in one direction, pause, rock in the other direction, etc. It assures that the capacitor across the timer relay has achieved full charge regardless of the setting of R1.

2. With this "long running time" program operating, adjust the appropriate potentiometers (see figure) for a good abrupt stop in either direction over the entire reel.

3. Run the same program, but with the running times changed to 120 milliseconds, to just barely get started before commanding a stop (which should last for one second as above) and adjust the appropriate short running time pot for good stop time. Repeat Steps 1 and 2 for check.

CORRECTIVE MAINTENANCE

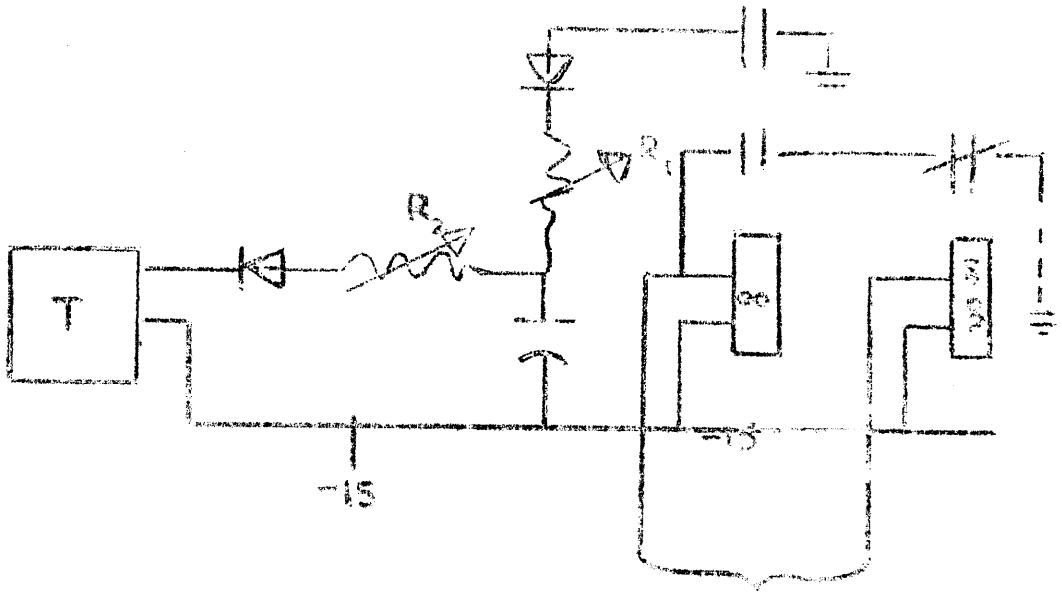
The equipment is constructed of highly reliable transistorized modules. Use of these circuits and faithful performance of the preventive maintenance tasks ensure relatively little equipment down time due to failure. Should a malfunction occur, the condition should be analyzed and corrected as indicated in the following procedures. For corrective maintenance no special tools or test equipment are required other than a broad bandwidth oscilloscope and a standard multimeter.

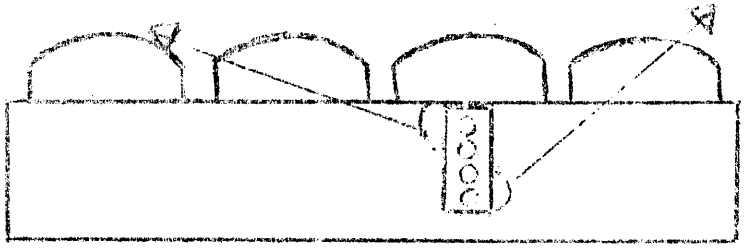
Troubleshooting Random Information Errors

A check for strobe timing is a good first step when troubleshooting random information errors. The position of the TP1 pulse generated from the timing track with respect to the information located on the information tracks determines the margins the system has for skew and amplitude variations. The TP1 (or strobe) should be centered on the information contained in the information channels (Figure 8). Unfortunately, this centering is primarily a function of parameters which are not controlled in the field. The main factors are: the gap width of the head, the velocity of the tape, and the switching time of the head.

To a lesser extent, however, the write current, tape tension, and the delays present in the reader and the writer do affect the strobe time.

The method for doing this is to use a scope with a high gain differential preamplifier such as a Tektron'x Type D or E. Also needed is a shielded cable with clip leads to connect the preamplifier to the tracks under consideration. The method is to look at any particular information channel and sync on the timing track TP1's, or with a dual beam scope, look at both the timing track output and this information signal. It is possible to see a bit of noise reflected onto the input of the information amplifiers because of timing pulses occurring at the output. This noise too, gives a good clue as to when the signal is being strobed.





Adjust upper potentiometer of pair (RZ) with long run time. Adjust lower potentiometer of pair for short run time. Turn all potentiometers clockwise, for clockwise for longer stop pulse = more abrupt stop

At the outset, the delay through the timing track amplifier should be measured and allowed for by checking the zero crossing of the input to the timing track amplifier and those at its output. If the output wave form is not of 50% duty cycle or if the two sides do not switch simultaneously for low level signals (use the attenuation plug to check) the timing track Read amplifier knobs may have to be adjusted. It has never been necessary, however, to adjust these in the field. The time delay of the reader amplifier should be subtracted from the time delays observed in the next part of the procedure to achieve an honest appraisal of when the output of the information chart amplifiers will be strobed.

Interpreting the results:

Result	Corrective Procedure
Get too large a carriage return Right current too big carriage return Head too fast carriage return Tape too slow	Strobe late when reading in the same direction as written and Strobes early when reading in opposite direction
Timing track read amplifer delay too large	Strobes late in either direction

Circuit Troubleshooting

The procedure followed for troubleshooting and correcting the cause of faults within specific circuits depends upon the down time limitations of equipment use. Where down time must be kept at a minimum, it is suggested that a provisioning parts program be adopted to maintain one spare module or standard component which can be inserted into the cabinet when system troubleshooting procedures have traced the fault to a particular component. Following is a list of this type:

Module No	Spares Per Central
4606	2
4223	1
4251	1
4523	2
4260	1

Bench troubleshooting procedures can then be performed to correct the defective components. Where down time is not critical, the spare parts list can be reduced and signal tracing techniques can be utilized to troubleshoot modules within the equipment. This practice

involves module removal by means of a Type 1960 System Module Puller, insertion of a Type 1954 System Module Extender into the logic rack, insertion of the suspect module in the module extender, and oscilloscope signal tracing of the module with the equipment energized and operating.

Static and dynamic circuit troubleshooting procedures may be performed at a bench. Visually inspect the module on both the component side and the printed-wiring side to check for short circuits in the etched wiring and for damaged components. If this inspection fails to reveal the cause of trouble or confirm a fault condition observed, use the multimeter to measure resistances.

CAUTION

Do not use the lowest or highest resistance ranges of the multimeter when checking semi-conductor devices. The X10 range is suggested. Failure to heed this warning may result in damage to components.

Measure the forward and reverse resistances of diodes. Diodes should measure approximately 20 ohms forward and more than 1000 ohms reverse. If readings in each direction are the same, and no parallel paths exist, replace the diodes.

Measure the emitter-collector and emitter-base resistances of transistors. Most catastrophic failures are due to short circuits between the collector and the emitter or are due to an open circuit in the base-emitter path. A good transistor indicates an open circuit in both directions between collector and emitter. Normally 50 to 100 ohms exist between the emitter and the base or between the collector and the base in the forward direction, and open-circuit conditions exist in the reverse direction. To determine forward and reverse directions a transistor can be considered as two diodes connected back-to-back. In this analogy PNP transistors are considered to have both cathodes connected together to form the base and both the emitter and collector assume the function of an anode. In NPN transistors the base is assumed to be a common-anode connection and both the emitter and collector are assumed to be the cathode.

Multimeter polarity must be checked before measuring resistances since many meters (including the Triplett 630) apply a positive voltage to the common lead when in the resistance mode. Note that although incorrect resistance readings are a sure indication that a transistor is defective, correct readings give no guarantee that the transistor is functioning properly. A more reliable indication of diode or transistor malfunction is obtained by using one of the many inexpensive in-circuit testers commercially available.

Damaged or cold-solder connections can also be located using the multimeter. Set the multimeter to the lowest resistance range and connect it across the suspected connection. Poke at

the wires or components around the connection, or alternately rap the module lightly on a wooden surface, and observe the multimeter for open-circuit indications.

Often the response time of the multimeter is too slow to detect the rapid transients produced by intermittent connections. Current interruptions of very short durations, caused by an intermittent connection, can be detected by connecting a 1.5-volt flashlight battery in series with a 1500-ohm resistor across the suspected connection. Observe the voltage across the 1500-ohm resistor with an oscilloscope while probing the connection.

Dynamic bench testing of modules can be performed through the use of special equipment. A Type 922 Test Power Cable and either a Type 722 or Type 765 Power Supply can be used to energize a systems module. These supplies provide both the +10 vdc and -15 vdc operating supply for the module as well as ground and -3 volt sources which may be used as signal inputs. The signal inputs can be connected to any terminal normally supplied by logic level by means of eyelets provided on the power cable. Type 911 Patch Cords may be used to make these connections between eyelets on the plug. In this manner logic operations and voltage measurements can be made. When using the Type 765 Bench Power Supply, marginal checks of an individual module can also be obtained.

Repair

In all soldering and unsoldering operations in the repair and replacement of parts, avoid placing excessive solder or flux on adjacent parts or service lines. When soldering semi-conductor devices (transistors, crystal diodes, and metallic rectifiers) which may be damaged by heat, the following special precautions should be taken:

a. Use a heat sink, such as a pair of pliers, to grip the lead between the device and the joint being soldered.

b. Use a 6-volt soldering iron with an isolation transformer. Use the smaller soldering iron adequate for the work.

c. Perform the soldering operation in the shortest possible time, to prevent damage to the component and delamination of the module etched wiring.

When any part of the equipment is removed for repair and replacement, make sure that all leads or wires which are unsoldered, or otherwise disconnected, are legibly tagged or marked for identification with their respective terminals. Replace defective components only with parts of equal or greater quality and tolerance.

SECTION 6

PERTINENT DOCUMENTS

PUBLICATIONS

The following documents serve as source material and complement the information in this manual. These publications may be obtained from the nearest Digital office or from:

Customer Relations Department
Digital Equipment Corporation
146 Main Street
Maynard, Massachusetts

a. Digital Modules Catalog, A-705. This book contains information pertaining to the function and specifications for the basic modules and accessories comprising the Microtape Control Type 550.

b. Microtape brochure, F-03-550, presents a general description of the Microtape system.

c. PDP-4 Handbook, F-45A, gives programming information for Microtape used with the PDP-4.

d. PDP-1 Handbook, F-15D, gives basic IOT programming information.

e. Silicon Modules 6000 Series, C-6000, describes the specifications and functions of Digital's silicon system modules.

LIBRARY PROGRAMS

The following programming brochures are available now and may be ordered from the Digital Program Library at the address given above.

PDP-4 Programs

a. Microtrieve, 4-29-10, allows the programmer to save areas of memory on on Microtape and quickly retrieve such information using the toggle switches on the PDP-4.

b. Microtog, 4-46-10, describes various programs to detect any errors in Microtape control.

c. Microtape Subroutines, 4-45-10, are programs which allow the programmer to read, write, or search the Microtape using prewritten and tested subroutines.

PDP-1 Programs

a. Microtape Control PGM, 1-26-IO, is a subroutine which transfers data to or from Microtape.

b. Microtape Format Pack, 1-127-IO, writes the mark track, timing track, and block numbers from 0 to 1077_8 on tape. It also allows the operator to check the tape after it was written.

c. Data Transfer Test, 1-128-IO, enables the operator to check data transfer to and from the computer and the Microtape control. This program also indicates which flags are being detected during the test.

d. Microtape Rocker Program, 1-129-IO, allows the user to oscillate tape over a desired area for debugging purposes.

e. Microtape Exerciser, 1-130-IO, evaluates the performance of Microtape and determines the nature of any errors that might occur.

f. Microtape Dump and Retrieve, 1-131-IO, allows the operator to store data on Microtape or retrieve data from Microtape using the TEST WORD switches.

g. Error Message, 1-132-IO, functions with a Microtape control to type out errors on the on-line typewriter.

ENGINEERING DRAWINGS

Engineering drawings in the following list are supplied with each Microtape system as an aid to understanding and maintaining the control and transport.

Module Schematics

RS-1011	Diode
RS-1105	Inverter
RS-1802	Relay
RS-4102	Inverter
RS-4105	Inverter
RS-4113	Diode
RS-4114	Diode
RS-4115	Diode
RS-4116	Diode
RS-4117	Diode
RS-4127	Capacitor-Diode-Inverter

Model Schematics (continued)

RS-4129	Capacitor-Diode-Inverter
RS-4151	Binary-to-Octal Decoder
RS-4202	Dual Flip-Flop
RS-4214	Quadruple Flip-Flop
RS-4218	Quadruple Flip-Flop
RS-4221	6-Bit Shift Register
RS-4228	3-Bit Shift Register with Buffer Register
RS-4260	Mark Track Decoder
RS-4261	Block Format Decoder
RS-4301	Delay
RS-4303	Integrating One-Shot
RS-4401	Clock
RS-4410	Pulse Generator
RS-4523	Manchester Reader and Writer
RS-4604	Pulse Amplifier
RS-4605	Pulse Amplifier
RS-4606	Pulse Amplifier
RS-4672	BCD Light Driver
RS-4680	Solenoid Driver
RS-6102	Inverter

Logic

BD-D-550-0-BD	Block Diagram, 550 Control
BS-D-550-0-C1	Control Print 1
BS-D-550-0-C2	Flag Response Data Control Outputs
BS-E-550-0-IN	In Information Handling
BS-D-550-0-TM	TM Control Pulses
BS-D-550-0-W	W Mark Track Decoding Error
TD-D-550-0-TD	Timing Diagram

Module Location and Wiring

UAL-D-555-0	Utilization Module List
WL-A-550-0-2	Logic Wiring (42 Sheets)
CL-A-550-0-3	Cable List (9 Sheets)
PW-A-550-0-4	Power Wiring
WL-A-550-0-9	Ground (4 Sheets)
CW-D-25326	Chassis Wiring for Type 555 Transport

BLOCK DIAGRAM

TAPE CONTROL 550